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positioning



REV 1.2

Technical Interface Description

uPatch102 GPS Receiver

This document describes the mechanical and electrical interfaces of the uPatch102 GPS receiver module.

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Fastrax Ltd.

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COMPLEMENTARY READING

The following reference documents are complementary reading for this document:

Ref. #	File name	Document name
(1)	CXD2951_communication_command_spc.pdf	CXD2951 Communication Command Specification version 1.8
(2)	CXD2951_communication_command_spc.pdf	CXD2951 Communication Command Specification version 1.7
(3)	CXD2951_Application_Note_EN.pdf	CXD2951 Application Note
(4)	uPatch100 and uPatch102 Plastic Holder Specifcation	uPatch100 and uPatch102 Plastic Holder 1.0.pdf

1. SYSTEM DESCRIPTION

1.1 General Description

A complete OEM GPS receiver with is implemented on the uPatch102 module. It is based on Sony GPS single chip receiver.

uPatch102 is intended as a pin-compatible replacement for Fastrax' uPatch100 range of products. The only hardware difference to uPatch100 is that uPatch102 has two additional I/O-pins for selecting the baud rates.

uPatch102 internal ROM code complies to SONY ASCII protocol version 1.8 (using SONY CXD2951-GL4 single chip LSI) whereas uPatch100 complies to SONY ASCII protocol version 1.7 (using SONY CXA3355 RF and CXD2956AGL-1 BB). See References (2) and (1) for further details.

NOTE! uPatch102 is only available from the factory in 4800 baud version. In case other baud rates are needed, then use the Baud rate Select pins.

uPatch102 comes in two different versions:

- **uPatch102C** – CMOS version for serial data
- **uPatch102R** – RS232 version for serial data

The default baud rate in both versions is 4800 baud.

The module includes the following features:

- 28 x 28 x 7.7 mm PCB form factor (4mm antenna version)
- 28 x 28 x 5.7 mm PCB form factor (2mm antenna version)
- Sony GPS: CXD2951GL-4 single chip
- Two external, regulated power supplies needed
- 10-pin interface on pad-row w/ 1.27mm pitch
- Valid fix indication output
- Pulse per second (PPS) output
- Internal POR and regulator circuitry

- Internal 32768Hz RTC
- Internal 18.414MHz TCXO
- WAAS/EGNOS compatible

1.2 Antenna Considerations

The uPatch102 includes an integrated high performance 25x25x4mm passive patch antenna which is tuned to 1578MHz on the 28x28mm GND plane. It is tuned on purpose 3MHz above L1 center frequency (1575MHz) in order to compensate the detuning effect of typical plastic covers or housings. Usually plastic covers shift the resonance frequency of the antenna downwards when it is placed closed to the antenna element.

uPatch102 is also available with a 25x25x2mm antenna element upon request.

Please contact Fastrax for further information about antenna tuning issues if needed.

1.3 Physical specification

- Size (incl. 4mm antenna):28.0 x 28.0 x 7.7mm [W x L x H]
- Size (incl. 2mm antenna):28.0 x 28.0 x 5.7mm [W x L x H]
- Weight: 12 g
- Operating Temperature: -40 °C to +85 °C
- Operating Humidity: 0% to 95% RH, non condensing
- Vibration 1 G

1.4 Technical specification

uPatch102 OEM GPS Receiver Module Specifications		
General:	L1 frequency, C/A code (SPS) 12 channels, WAAS/EGNOS compatible Integrated antenna receiver Separate search and acquisition engine	I/O ports: One serial data port 10-pin interface pads Two Baud Rate Select pins 1PPS output Valid fix indicator output Main power supply External Reset input Battery backup supply
Update rate:	1 fix/s	Protocol: NMEA 0183 ver 3.0 SONY ASCII
Accuracy:	Position: 3m (CEP), 6m 2dRMS Velocity: 0.1 m/s Time: 50ns RMS	Dimensions: 28mm x 28mm x 7.7m (nominal) 28mm x 28mm x 5.7m (nominal)
TTFF:	Cold Start: 45s typical Warm Start: 35s typical Hot start: 8s	Weight: 12g
Sensitivity:	Acquisition (unaided): -139dBm Tracking: -152dBm Navigation: -150dBm	Operating voltage: 3.3V..5.5V (main supply) 2.5V..5.5V (battery backup supply)
Power Drain (3.3V):	Acquisition: 81-90mA (max) Navigation: 47-53mA (average) Battery backup <20uA (Battery backup mode) Battery backup <300uA (Normal mode)	Operating temperature: -40C..+85C
		Antenna: 25x25x4mm or 25x25x2mm
		GPS Receiver IC: CXD2951GL-4 Single Chip

The current consumption is different in different modules. The following table summarizes them:

Model	Average (navigation)	Max (acquisition)
uPatch102-C	47 mA	81 mA
uPatch102-R	53 mA	90 mA

The battery backup current is <20uA in all modules at room temperatures (VDD removed). Battery backup current increases slightly with temperature. The current drawn by the VBAT pin is also higher in normal operation mode (VDD powered) due to internal SRAM read/write operations.

Maximum VBAT current is however always <300uA. Worst case is at +85deg in normal operation mode when internal SRAM, which is powered by battery backup supply, is dynamically accessed.

1.5 Block diagram

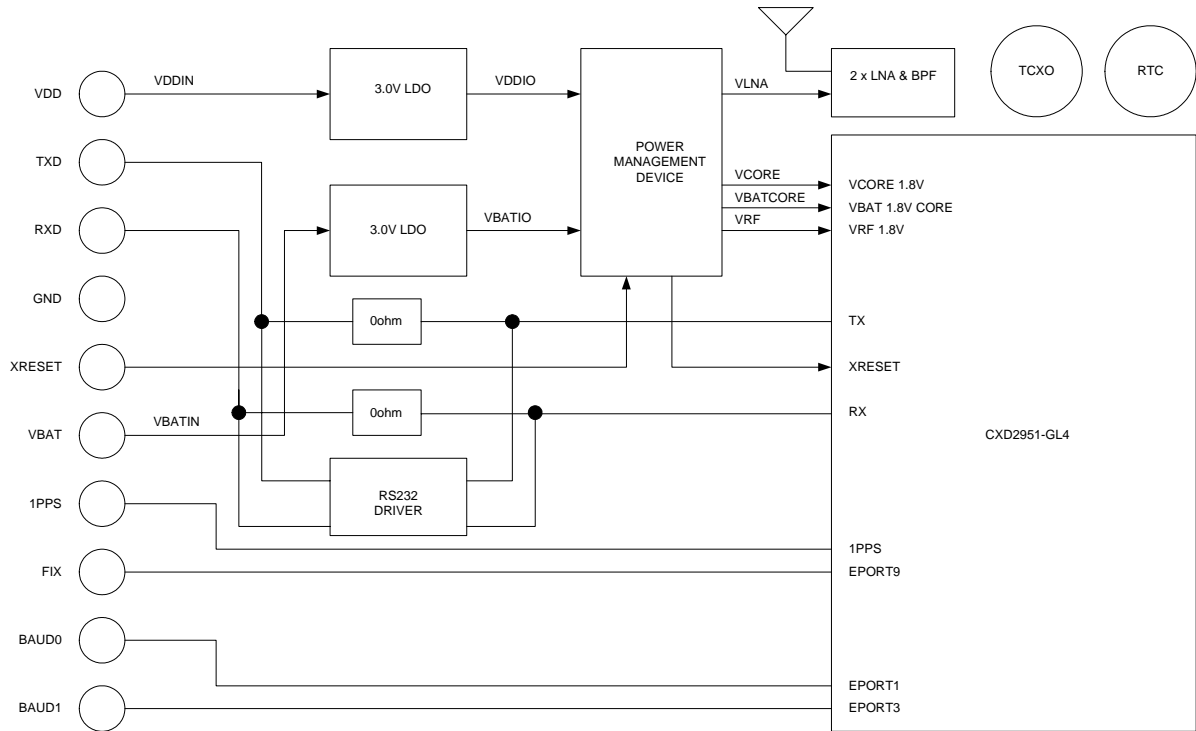


Figure 1 Block diagram of uPatch102 GPS receiver

1.6 Pictures of uPatch102



Figure 2 UPatch102 module

1.7 2D versus 3D positioning

The uPatch100-S calculates a 2D fix whenever possible using 3 satellites and a 3D fix using 4 or more satellites. 2D fix is calculated also at Cold Start. The following DOP limitations apply:

- PDOP \leq 20
- HDOP \leq 20

1.8 WAAS/EGNOS Compatibility

uPatch100-S is WAAS/EGNOS compatible. One acquisition and tracking channel is always reserved for WAAS/EGNOS tracking. See reference (3) for details of WAAS usage.

Note! EGNOS is still in test phase and is not used for corrections.

2. MECHANICAL DIMENSIONS

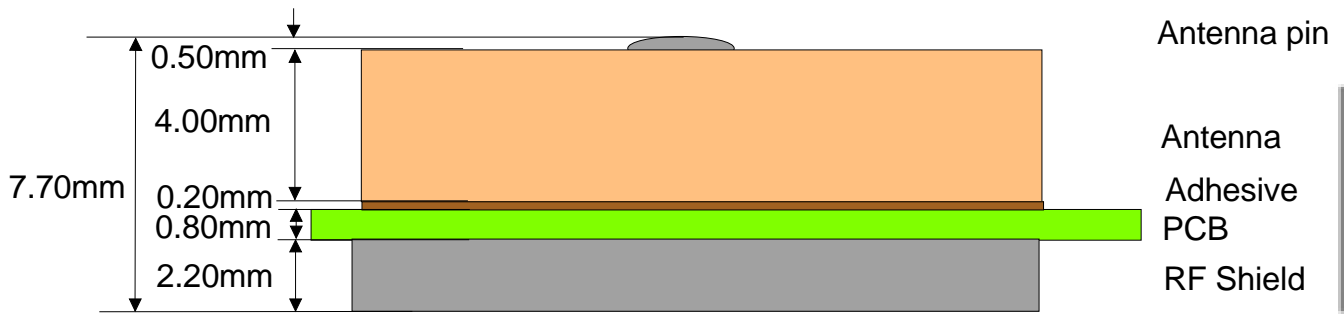


Figure 3 uPatch102 mechanical outlines

Nominal height is 7.7mm. Max height is 7.9mm including tolerances.

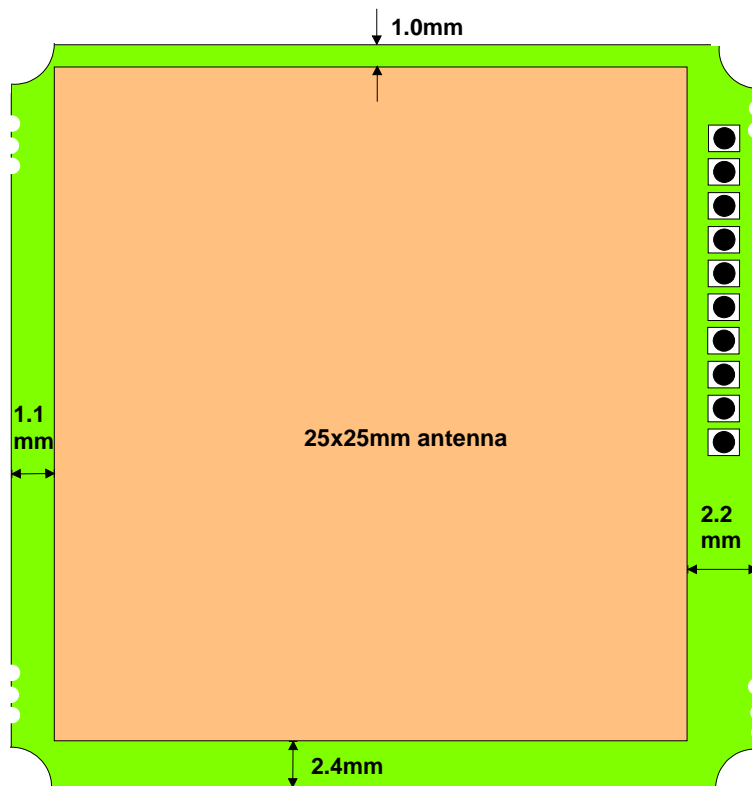
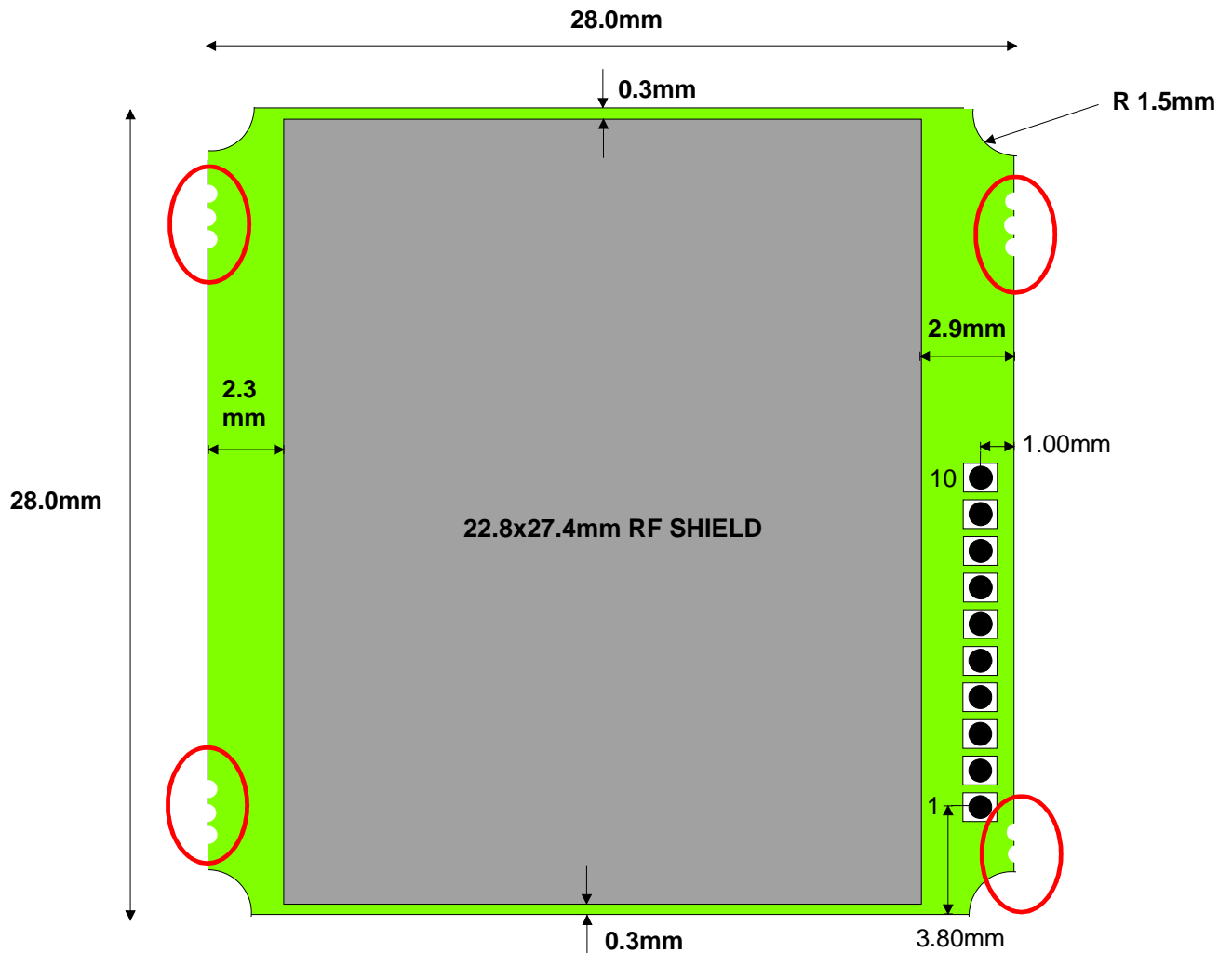


Figure 4 uPatch102 mechanical outlines – top view

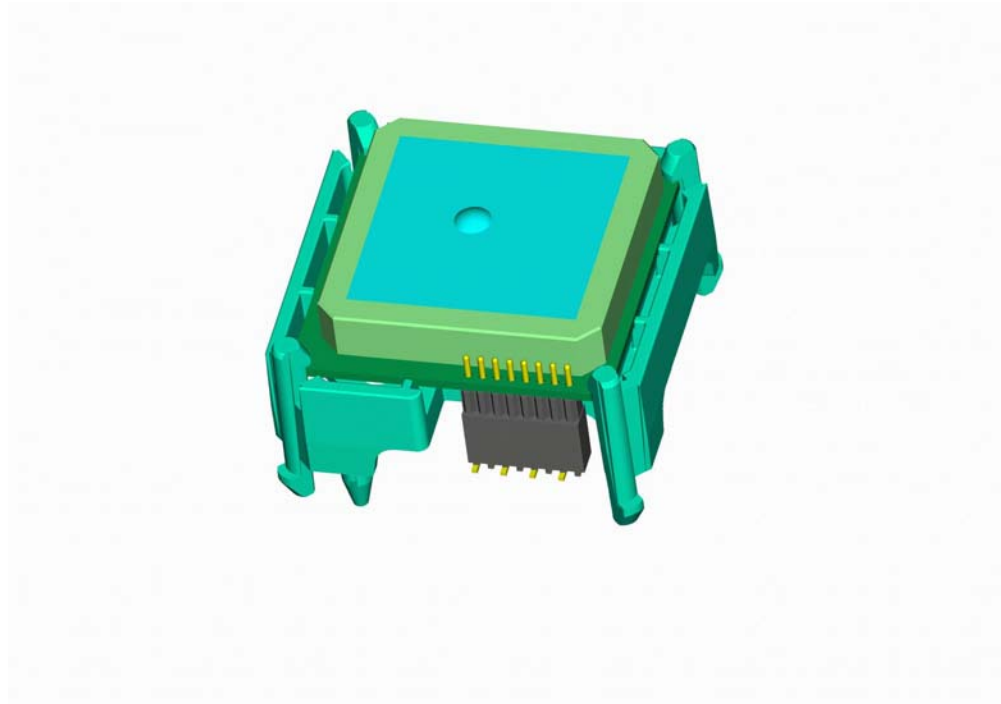


 INDICATES PANEL CUT-OUT DRILL HOLES. SOME RESIDUALS MAY BE LEFT AFTER REMOVAL FROM PANEL

Figure 5 uPatch102 mechanical outlines – bottom view

PCB dimensions are nominally 28x28mm. Please note that some PCB residuals can be left over when removed from panel. Please see figure above.

Fastrax offers a plastic holder for attachment to customer PCB. Please refer to reference (4) for details.



A suitable interface cable is for instance Flexstrip from Tyco Electronics (www.tycoelectronics.com).

When ordering Flexstrip please specify the following:

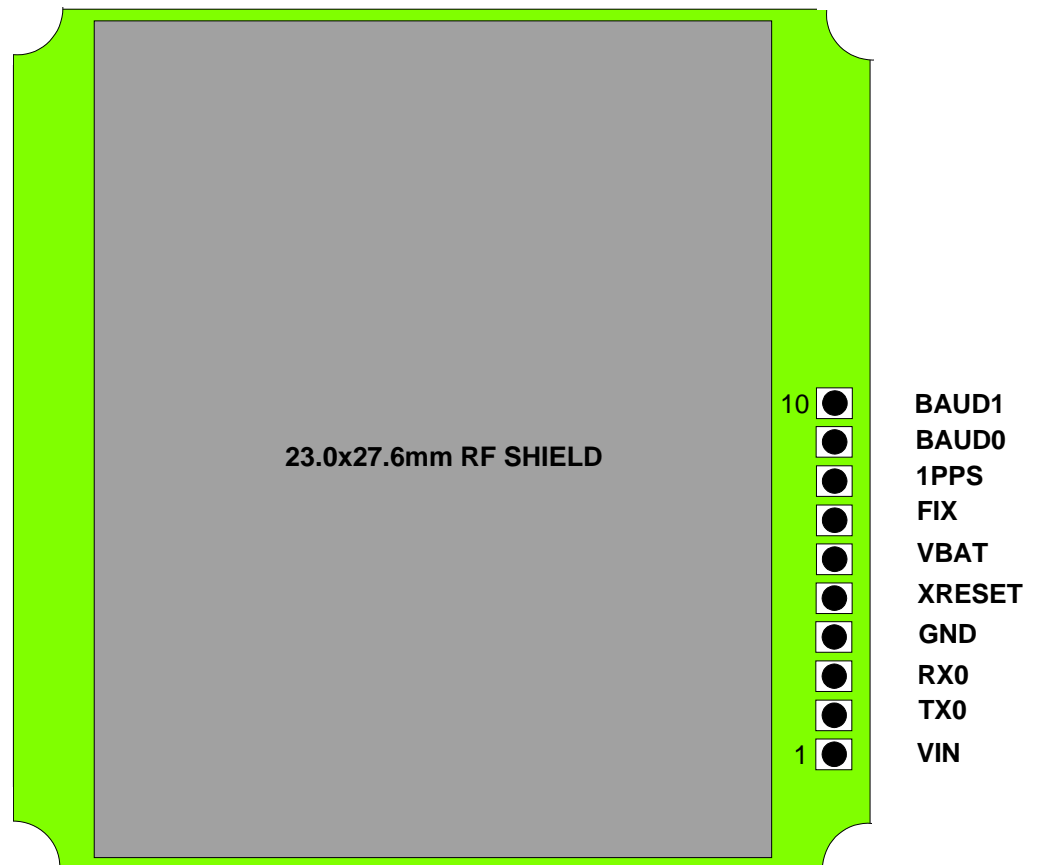
- Insulation Material
- Pitch
- Insulation length
- Termination on both sides
- Number of conductors.

An example of a cable is FST-13A-8, i.e. FS = FlexStrip, T = Teflon insulation, 1 = 1.27mm pitch, 3 = 76.3mm Insulation length, A = straight termination and 8 = 8 conductors.

3. EXTERNAL INTERFACES

3.1 System connector

The system interface consists of a 10-pin SMD pad row on one edge of the PCB. The module is suitable for connecting using a 10-pin header.



The following signals are available in the system connector for uPatch102C version:

uPatch102-C Pin-out			
Pin	Name	I/O	Description
1	VDD	PWR	Main Supply (3.3V...5.5V)
2	TX0	O	NMEA Output, 3.0V CMOS level
3	RX0	I	SONY ASCII Input, 3.0V CMOS level
4	GND	GND	Ground
5	XRESET	I	External Reset, Active Low
6	VBAT	PWR	Battery Backup Supply (3.3V...5.5V)
7	1PPS	O	1 Pulse Per Second Output
8	FIX	O	Valid Fix Indicator Output
9	BAUD0	I	Baud Rate Select 0 Input
10	BAUD1	I	Baud Rate Select 1 Input

The following signals are available in the system connector for uPatch102R version:

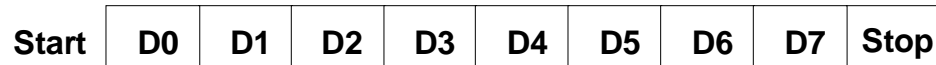
uPatch102-R Pin-out			
Pin	Name	I/O	Description
1	VDD	PWR	Main Supply (3.3V...5.5V)
2	TX0	O	NMEA Output, RS232 level
3	RX0	I	SONY ASCII Input, RS232 level
4	GND	GND	Ground
5	XRESET	I	External Reset, Active Low
6	VBAT	PWR	Battery Backup Supply (3.3V...5.5V)
7	1PPS	O	1 Pulse Per Second Output
8	FIX	O	Valid Fix Indicator Output
9	BAUD0	I	Baud Rate Select 0 Input
10	BAUD1	I	Baud Rate Select 1 Input

3.2 UART interface

One asynchronous UART port is available for serial interfacing. The data format is : xxxx,N,8,1, i.e. 4800/9600/19200 or 38400 baud, no parity, eight data bits and 1 stop bit (baud rate is externally configurable using Pins 9 (BAUD0) and Pin 10 (BAUD1)). Note! The receiver has an internal pull-up (15kohm) on pin BAUD0 and an internal pulldown (100kohm) on BAUD1 so in case 4800 baud is ok then the inputs can be left unconnected.

<4.7kohm drive impedance is needed for BAUD0 and BAUD1 external control.

No other data formats are supported. LSB is sent first.



Parity: N
Data Bits: 8
Stop bits: 1

Figure 6 UART Data format (3.0V CMOS levels).

The UART port is named PORT0. PORT0 is used for NMEA 0183 output (TXD0) and system command input using Sony ASCII protocol (see reference (1) for details) through RXD0 in normal operation.

NOTE

The RS232 driver in uPatch102-R goes to automatic shutdown if RXD0 is floating (=> no TXD0 data coming out). If RXD0-pin is not used by the application it must be connected to VDD.

3.3 FIX Output (Valid Fix Indicator Output)

Status output is dedicated for valid fix indication. See timing diagram below for different modes.

During signal acquisition phase the Pin 12 toggles with a 0.5Hz duty cycle (i.e. 1 second high, 1 second low)

During signal tracking phase (Navigation message decoded from at least one satellite) the Pin 12 toggles with a 1Hz duty cycle (i.e. 0.5 second high, 0.5 second low).

A valid fix is indicated with a high level signal.

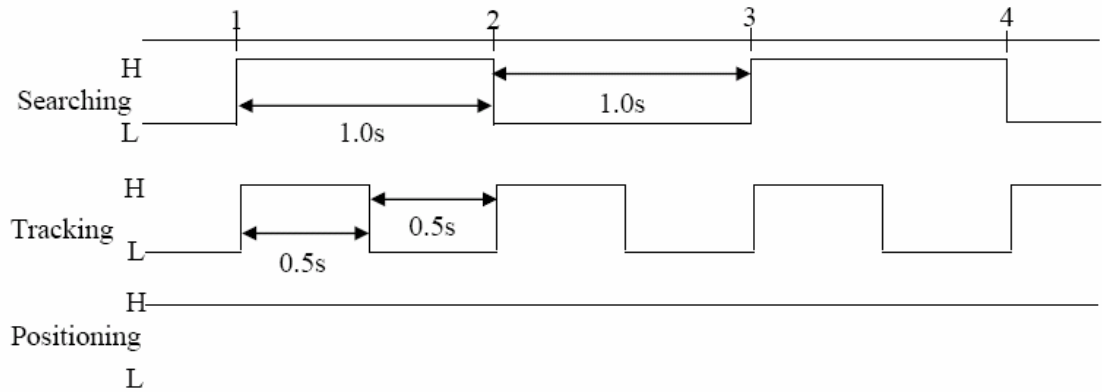


Figure 7 Valid fix indicator output in different modes.

Note that the current sourcing capability of FIX output is only 4mA. An external buffer is needed for driving e.g. a LED.

3.4 Baud Rate Select Interface pins

The baud rate can be selected externally using BAUD0 and BAUD1 pins according to the table below.

Baud Rate	BAUD0	BAUD1	NMEA Messages
4800	HIGH	LOW	GPGGA, GPGSA, GPGSV, GPRMC
9600	LOW	LOW	GPGGA, GPGSA, GPGSV, GPRMC, GPVTG, GPZDA, PSGSA
19200	LOW	HIGH	GPGGA, GPGSA, GPGSV, GPRMC, GPVTG, GPZDA, PSGSA
38400	HIGH	HIGH	GPGGA, GPGSA, GPGSV, GPRMC, GPVTG, GPZDA, PSGSA

The default NMEA messages at different baud rates are also shown in the table above. The user can customize the NMEA sentences using the @NC command as described in Reference (1).

3.5 XRESET Input

uPatch102 includes an internal POR (Power-On-Reset) device. The POR device has an option for providing an external RESET pulse (active low). If this external XRESET functionality is not used then the XRESET pin can be left unconnected.

3.6 Power supply interfaces

There are two external power supply inputs available (VIN and VBAT).

VIN input is the main power supply input supplying the GPS receiver RF and base-band sections. On board regulators provides the internal supply voltages. A internal Power-On-Reset (POR) circuit is also available that monitors the VIN supply. The POR circuit provides an active low RESET (held 300ms low) signal to the base-band device once the VIN has reached proper voltage level.

VBAT input is dedicated for supplying the receiver in battery backup mode. On board regulator provides the internal battery backup supply voltage (1.8V).

In normal operation both power supplies (VIN and VBAT) should be supplied with a regulated voltages.

For low power mode (battery backup mode) the VIN supply can be removed at any time. VBAT provides supply voltages to the battery backup sections of the receiver keeping the RTC running and the battery backed-up section of SRAM alive.

NOTE

The uPatch102 will not operate without the VBAT supply as it supplies power to the RTC section. See section 5 for details.

3.8 1PPS Output

The 1PPS output provides a timing pulse synchronized to GPS time once a valid fix is available.

The figure below shows the behavior of 1PPS output signal after Power On Reset. For a period of 160us after RESET the 1PPS signal

outputs the system clock frequency/3. 500ms after RESET the actual 1PPS signal is activated.

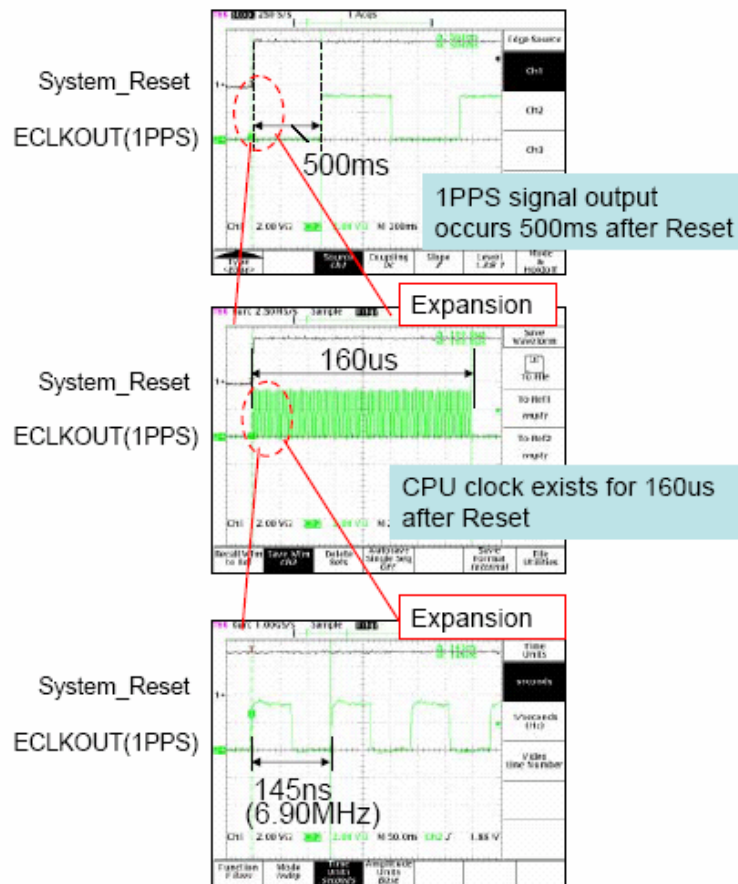


Figure 8 1PPS signal output after RESET

4. PROTOCOLS

4.1 SONY ASCII Protocol

The uPatch102 can be customized using the SONY ASCII Protocol on Port 0. A detailed explanation of the commands can be found in Reference (1).

4.2 NMEA Protocol

UPatch102 can output 8 different NMEA sentences on Port 0: GPGGA, GPGLL, GPGSA, GPGSV, GPRMC, GPVTG, GPZDA and PSGSA. In order to customize the output sentences the SONY ASCII protocol command @NC must be used. See Reference (1) for details.

The default NMEA messages are:

4800: GPGGA, GPGSA, GPGSV and GPRMC

9600: GPGGA,GPGSA,GPGSV,GPRMC,GPVTG,GPZDA,PSGSA

19200: GPGGA,GPGSA,GPGSV,GPRMC,GPVTG,GPZDA,PSGSA

38400: GPGGA,GPGSA,GPGSV,GPRMC,GPVTG,GPZDA,PSGSA

Note that at 4800 baud less than 6 messages can be output.

Note also that NMEA messages are retained if the receiver has battery backup connected. A reset does not clear the NMEA mask so if the receiver is configured for 4800 baud and then changed to i.e. 9600 baud with the battery backup active the baud rate is changed accordingly but the NMEA mask remains. This can be cleared with the @clr command or removal of battery backup.

5. APPLICATION NOTE FOR POWER SUPPLIES

The uPatch102 has two separate power supply inputs; VDD and VBAT. In normal operating mode power is supplied to both of them. Note that VBAT must be powered in order to keep the RTC running and the receiver in operation.

There are however customer cases where to separate supplies are not available. The following sections shows different power supply possibilities.

NOTE

Note that the dynamic current consumption from VBAT can be upto 300uA @ +85deg! In battery backup mode the current consumption of VBAT is however in the <20uA range.

4.1 Separate VDD and VBAT supplies available

The best performance combined with low power operating modes are achieved with two separately controlled power supplies; one for VDD and one for VBAT. It is also the most cost efficient solution.

In this mode VDD can be turned off anytime and the receiver then enters sleep mode leaving the RTC and some portion of the internal SRAM powered from VBAT. When VDD is turned on the receiver resumes normal operation and if the ephemeris are still valid it performs a Hot Start. If the ephemeris are old it performs a Warm Start.

If both VDD and VBAT are removed all data is lost and the receiver performs a Cold Start once powered up again. Note that the receiver cannot operate without VBAT.

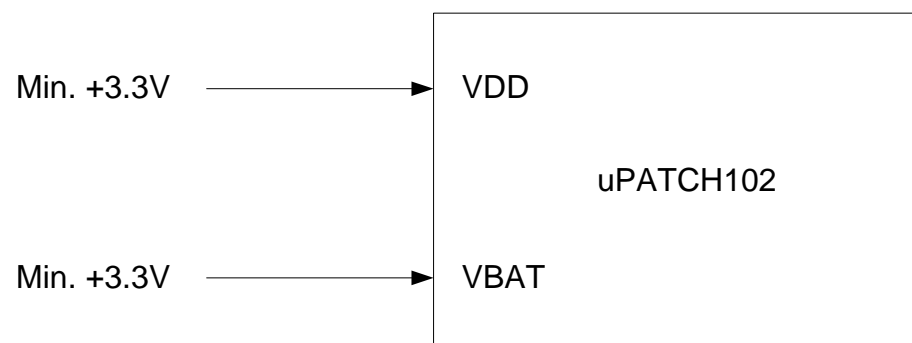


Figure 9 uPatch102 powered with two separate supplies

4.2 Single supply available

If only one supply is available then it should be connected to both VDD and VBAT. In this way no low power modes can be achieved as the receiver is continuously running. The following figure show the connection.

When the power supply is removed all information is lost (Time, Last Known Good Position, Satellite Ephemerides etc.). Once powered up again the receiver performs a Cold Start.

Note that VBAT must also be connected in order for the receiver RTC operational.

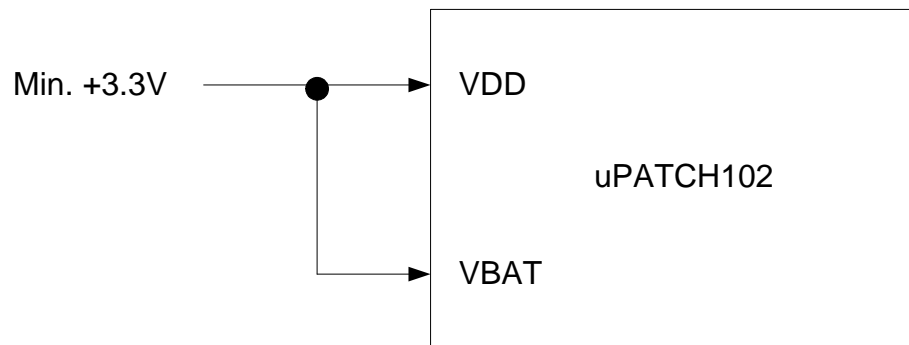


Figure 10 uPatch102 powered with one single external supply

4.3 Single supply using Super Cap for VBAT

An external high capacity capacitor can also be used for VBAT supply if only one power supply is available. The recommended circuitry is shown in the figure below. The diode should be of Schottky type with a very low drop-out voltage (typically 150mV). The capacitor can be e.g. a 1F 5.5V.

In this way the VDD can be removed at any time. The receiver operates in the same mode as described in section 4.1.

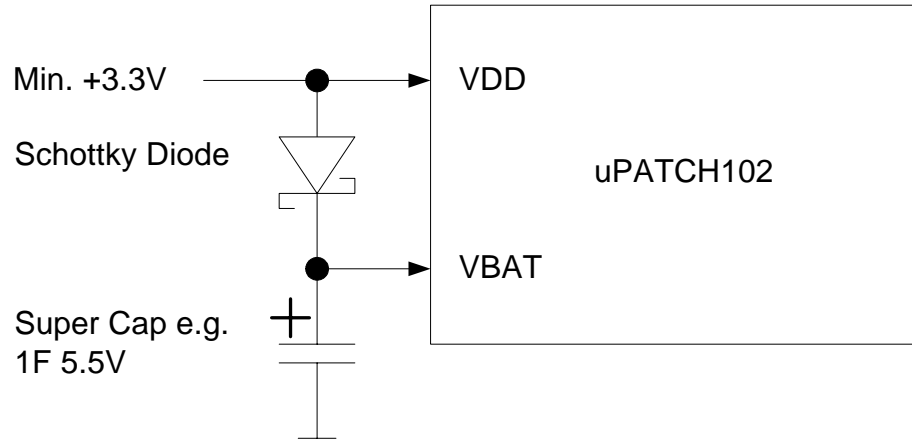


Figure 11 uPatch102 powered with one single external supply